IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: KRISHNAMOORTHY *et al.*	Art Unit: 2138
Appl. No.: 10/710,451	Examiner: TABONE JR.JOHN J
Filed: 07/12/2004	Attorney Docket No.: TI36271
For: Testing of Modules Operating With Different Characteristics of Control Signals Using Scan Based Techniques	

Declaration Under 37 CFR 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 223131450

Sir:

We, Nikila KRISHNAMOORTHY and Rubin Ajit PAREKHJI declare as follows:

1. We are the co-inventors of claims 1-14, as sought to be amended in the accompanying response to the outstanding office action dated 4/20/2006.

2. We were part of a design team for an integrated circuit referred to as 'Sangam' internally within Texas Instruments Incorporated (the assignee of the instant patent application) and later released into the market by a product code of TNETD 7300.

3. The roles of the three inventors of the instant patent applications were at least approximately as follows: (1) Mr. Rubin Parekhji was the lead engineer for Design for Testability (DFT) team for the Sangam Chip design; (2) Ms. Nikila Krishnamoorthy was a member of the DFT team; and (3) Mr. Anindya Saha was also a lead engineer responsible for the design of the chip.

4. On a day prior to August 8 2002, we both conceived of at least the invention of pending claim 1 (including any amendments submitted with the accompanying response). In particular, we both recall having discussion of the invention of pending claim 1. This is based on our recollection of the events, in addition to the timelines noted below.

5. On or around August 28 2002, as evidenced by the attached Exhibit A (redacted), we presented to the technical management team responsible for the design of the Sangam Chip a proposal to incorporate the changes necessitated by the implementation of the subject matter supporting at least pending claim 1.

6. On or around August 28 2002, the technical management team approved our proposal to incorporate the changes.

7. Between August 8 2002 and August 28 2002, we received a preliminary netlist for the Sangam chip, and decided to integrate at least the invention of pending claim 1 into the Sangam chip.

8. Between August 28 2002 and September 11 2002, we implemented the proposed changes, including at least the features of pending claim 1 at the design entry level in Register Transfer Level (RTL) code.

9. On or around September 11 2002, we entered the RTL code into a design database that was intended to store various information related to the Sangam Chip.

10. On or around December 30 2002, we released the design of the Sangam Chip, including at least the invention pending claim 1, for fabrication.

11. Between September 11 2002 and December 30 2002, we performed at least some of various tasks (as related to at least the usage and implementation of the features of pending claim 1) such as physical design, timing closure, device Automatic test pattern generation (ATPG) setup, pattern simulation in timing mode, which are generally required in the design of chips.

12. On or around February 3 2003, we received samples of the Sangam chip, and tests were conducted thereafter to confirm functionality, as evidenced by the Attached Exhibit B, which is an email communication from Mr. Suresh Kumar (Project design manager for the Sangam Chip) to the design team of the Sangam product. The tests

conducted at later stages included ATPG tests which successfully tested the features of pending claim 1.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

August 11, 2006
Date

Nikila KRISHNAMOORTHY
(Inventor)

August _____, 2006
Date

Rubin Ajit PAREKHJI
(Inventor)

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August , 2006
Date

Nikila KRISHNAMOORTHY
(Inventor)

August 04, 2006
Date

Rubin Ajit PAREKHJI
(Inventor)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 223131450

Sir:

I, Anindya SAHA, declare as follows:

1. I am a co-inventor of claims 1-14, as sought to be amended in the accompanying response to the outstanding office action dated 4/20/2006.

2. I was part of a design team for an integrated circuit referred to as 'Sangam' internally within Texas Instruments Incorporated (the assignee of the instant patent application) and later released into the market by a product code of TNETD 7300.

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so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

August 3rd, 2006
Date

Anindya SAHA
(Inventor)

Open Issues / Risks

- Implementation changes required in the top-level test logic due to scan-related issues in the MIPS and C62x cores.
  - Test clock inverted for C62x core to generate valid patterns in Fastscan.
  - Change in scan enable hookup for MIPS necessary due to clock-gating inside the core.
  - Issues with handling conditional captures in MIPS core.

Appli. No.: 10/710,451
Exhibit A (Page 1 of 1)

From: "Kumar, Suresh" <suresh@ti.com>
To: "isangam@list.ti.com - Sangam team in India" <isangam@list.ti.com>,
"isangam-ldrs@list.ti.com - TII BSTC SANGAM LEADERS"
<isangam-ldrs@list.ti.com>
Subject: FW: Sangam Silicon program weekly update. 2/3/03.
Date: Mon, 3 Feb 2003 11:11:00 +0530
MIME-Version: 1.0
X-Mailer: Internet Mail Service (5.5.2653.19)
Content-Type: multipart/alternative;
boundary="----_=_NextPart_001_01C2CB46.D514C9B6"
Sender: owner-isangam@list.ti.com
Precedence: bulk

------_=_NextPart_001_01C2CB46.D514C9B6
Content-Type: text/plain

Sangam status

- Suresh.

Appli.: 10/710,451
Exhibit B (Page 1 of 1)

... redacted...

* Lead lot came out Friday night. First two wafers were probed with very limited tests (MemBIST on all BISTED memories, BI pattern chain test, IDDQ, I/O Leakage, OPEN and SHORTS.

...

* ATPG showed some activity in device through capture-tool (graphical view of signal states), which matched expected results. However, an S/W issue has corrupted the patterns and even though results matched expected data, tester reported a failure. We feel the ATPG controller and the flip-flop chains are functional, but were unable to test with the Scan vectors due to this corruption problem. Debug stopped in favor of probing wafers as reported above and will be resumed on packaged units Monday morning. Analog test debug will also start with packaged units Monday morning.